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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/589,621	06/07/2000	Sara Ruhina Biyabani	004860.P2438	8620

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EXAMINER
CASCHERA, ANTONIO A

ART UNIT	PAPER NUMBER
2697	

DATE MAILED: 11/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/589,621	BIYABANI, SARA RUHINA	
	Examiner	Art Unit	
	Antonio A Caschera	2697	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 6/7/200 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

a. "...personal computer...", should read, "...personal computers..." (see page 9, line 2).

b. "...memory controller 207..." , should be replaced with "...memory controller 201..." (see page 11, line 8).

c. "Important change since the bandwidth for refresh rate is actually less than the bandwidth for frame formation," is an unclear sentence (see page 12, lines 9-10).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-3, 6, 9 and 15-19 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The element of the independent claims 1 and 15 where the applicant claims the memory controller operable for partitioning an address space for the color buffer in main memory into

two logical buffers is not described in the specification/drawings. Figure 2 comprises a main memory (#203) with a frame-preparation memory buffer (#205) contained therein along with a separate memory containing the refresh memory buffer (#207). The structure claimed in the above element found in claims 1 and 15 calls for two logical buffers including the refresh buffer in main memory. Neither the specification nor the drawings support the above element found in claims 1 and 15. Also, it is noted that claim 2, for example, contradicts this limitation of claim 1. For prior art rejections, this element will be interpreted as described in the specification and drawings such that one logical buffer is in the main memory and another is found separate from main memory.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 2 and 16 are unclear since they contradict the memory structure in their parent claims as to where the refresh memory is located. The memory structure claimed in parent claims 1 and 15 calls for two logical buffers including the refresh buffer in main memory where as claims 2 and 16 call for a refresh memory mapped into a dedicated memory separate from the main memory.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5, 10-12, 15-16, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stortz (U.S. Patent 5,900,885) in view of Asaro et al. (U.S. Patent 6,100,906).

In reference to claim 1, Stortz discloses a video memory architecture including a system memory controller connected via a bus to a system memory (see Figure 1 of Stortz, System Memory Controller (#15) connects to Memory (#14) via bus (#18)). Stortz discloses assigning an incremental video buffer in main memory and a decoupled video buffer in video memory (see Figure 2, reference #42a, 42b and column 2, lines 41-44). Stortz also discloses connecting the incremental video buffer to a graphics subsystem and connecting the video buffer to a display device (see Figure 1, Memory (#14) is connected to Video Controller (#20) via bus (#18) and DRAM (#22) is connected to Display (#24). Also see Figure 2, reference #42a, #42b). Stortz does not expressly disclose color data being written into the frame-preparation memory at a frame rate and read from the refresh memory at a rate that supports a refresh rate of the display device (though it does mention color data in column 1 lines 24-25, for example) however, Asaro et al. does. Asaro et al. discloses writing color data (see column 5, lines 25-28) to a first buffer to store produced data at a processing rate (see column 3, lines 1-13) and flipping the buffers at a refresh rate of the display (see column 1, lines 49-53 and column 2, lines 53-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the

main memory architecture of Stortz with the double buffering techniques as disclosed in Asaro et al. in order to break the dependency between software and hardware of many co-processing applications, including video graphics applications, thereby enabling the central processing unit to provide the data at a rate which is independent of the processing rate of the co-processor and/or the recipient processor (see column 3, lines 14-20 and column 2, lines 6-29 of Asaro et al.). Also, both references are directed to improvements in display systems.

In reference to claim 2, in addition to the teachings of all of the claim limitations as applied to claim 1 above Stortz discloses a video buffer located in video DRAM memory which is separate from the main memory (see Figure 2, Video Buffer (#42a) separated from incremental video buffer (#42b) in main memory (#14)).

In reference to claim 3, in addition to the teachings of all of the claim limitations as applied to claim 1 above Stortz discloses assigning an incremental video buffer in main memory and a decoupled video buffer in video memory (see Figure 2, reference #42a, 42b and column 2, lines 41-44). Stortz does not expressly disclose color data being copied from the frame-preparation memory to the refresh memory. Asaro et al. discloses writing color data to a first buffer color data (see column 5, lines 25-28). Neither reference expressly disclose data being copied from the frame-preparation memory to the refresh memory however, referring to Figure 2 of Stortz, in order for data to be displayed it must be transferred from Video Buffer (#42b) in Main Memory (#14) to Video Buffer (#42a) in the Video Controller (#20) which is then connected to a display device (see Figure 1, reference #22, 24) which meets the claim limitations.

In reference to claim 5, in addition to the teachings of all of the claim limitations as applied to claim 3 above Asaro et al. also discloses the method of switching the coupling between the processing module (see Figure 1, reference #20) and first/second buffers (#26,#28) and the coupling between first/second buffers and the recipient engine (#24) when the next frame of video data is read to be displayed (see column 4, lines 51-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to copy data using Stortz's methods above when switching buffer connections, as disclosed by Asaro et al., in order to allow for a continuous flow of data to be displayed diminishing the possibility of a visible separation of images, or tearing (see column 1, lines 46-49 of Asaro et al.).

Claims 10 and 15 are similar in scope to claims 1 and 3 and therefore are rejected under similar rationale.

Claims 11 and 16 are similar in scope to claim 2 and therefore are rejected under similar rationale.

Claims 12 and 18 are similar in scope to claim 5 and therefore are rejected under similar rationale.

5. Claims 4, 13, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stortz (U.S. Patent 5,900,885) and Asaro et al. (U.S. Patent 6,100,906) as applied to claims 3, 10, 15 above, in further view of Swan (U.S. Patent 6,304,297 B1).

In reference to claim 4, Stortz and Asaro et al. teach all of the claim limitations as applied to claim 3 above except for the copying of color data at pre-determined intervals. Swan discloses that it is conventional in a video graphics system to have a refresh rate of 60 hertz, producing and storing frames of video data in a frame buffer once every $1/60^{th}$ of a second (see

column 1, lines 24-28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Stortz and Asaro et al. above with the pre-determined timing disclosed by Swan in order to reduce the occurrences of drift such that an overflow or underflow condition results in a frame buffer (see column 1, lines 51-53 of Swan).

Claim 13 is similar in scope to claims 3 and 4 and therefore is rejected under similar rationale.

Claim 17 is similar in scope to claim 4 and therefore is rejected under similar rationale.

6. Claims 6-9, 14, 19, 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stortz (U.S. Patent 5,900,885) and Asaro et al. (U.S. Patent 6,100,906) as applied to claims 1, 10 and 15 above, in further view of Naughton et al. (U.S. Patent 5,519,825).

In reference to claim 6, Stortz and Asaro et al. teach all of the claim limitations as applied to claim 1 above except for the further partitioning of memory into a third buffer. Naughton et al. discloses a memory architecture where a third buffer, a cache buffer (see Figure 2, reference #125), is implemented in transferring data to the back buffer (#112) (see Naughton et al. column 6, lines 56-62 and Abstract, lines 8-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate a third buffer into the claimed memory architecture in order to optimize the copying of data from the third to the second/first frame buffers (see column 6, lines 57-60).

In reference to claims 7-9 and 21, Stortz and Asaro et al. teach all of the claim limitations as applied to claims 6, 7, 1 above except for implementing a third buffer for transferring data. Naughton et al. discloses a memory architecture where a third buffer, a cache buffer (see Figure

2, reference #125), is implemented in transferring data to the back buffer (#112) (see column 6, lines 56-62). In addition to the teachings of all of the claim limitations as applied to claims 1 and 6 above Asaro et al. also discloses a method of switching the coupling between the processing module (see Figure 1, reference #20) and first/second buffers (#26,#28) and the coupling between first/second buffers and the recipient engine (#24) (see column 4, lines 51-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the switching methods of Asaro et al. with the memory architecture of Naughton et al. in order to prevent "frame tears" or the case when motion from one frame to the next causes distortion in a graphic image presented on the display (see column 1, lines 59-63 of Naughton et al.)

In reference to claim 14, in addition to the teachings of all of the claim limitations as applied to claim 10 above, Asaro et al. also discloses the method of switching the coupling between the processing module (see Figure 1, reference #20) and first/second buffers (#26,#28) and the coupling between first/second buffers and the recipient engine (#24) when the next frame of video data is ready to be displayed (see column 4, lines 51-60). Naughton et al. discloses a memory architecture where a third buffer, a cache buffer (see Figure 2, reference #125), is implemented in transferring data to the back buffer (#112) (see column 6, lines 56-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the switching methods of Asaro et al. with the memory architecture of Naughton et al. in order to prevent "frame tears" or the case when motion from one frame to the next causes distortion in a graphic image presented on the display (see column 1, lines 59-63 of Naughton et al.)

Claims 19 and 20 are similar in scope to claims 6 and 7 and therefore are rejected under similar rationale.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Antonio Caschera whose telephone number is (703) 305-1391. The examiner can normally be reached Monday-Thursday and alternate Fridays between 7:00 AM and 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Mancuso, can be reached at (703)-305-3885.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

aac

10/28/02